OCXO Layout Guidelines

CONNOR WINFIELD

Application Note: AN2093

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Section 1: About this document.

1.1 Introduction

The techniques included in this application note will help to ensure successful printed circuit board layout using an oven-controlled crystal oscillator (OCXO). Problems with layout can result in noisy and distorted frequency transmissions, error-prone digital communications, latch-up problems, significantly reduced frequency stability, thermal instability within the OCXO, and other undesirable system behavior.

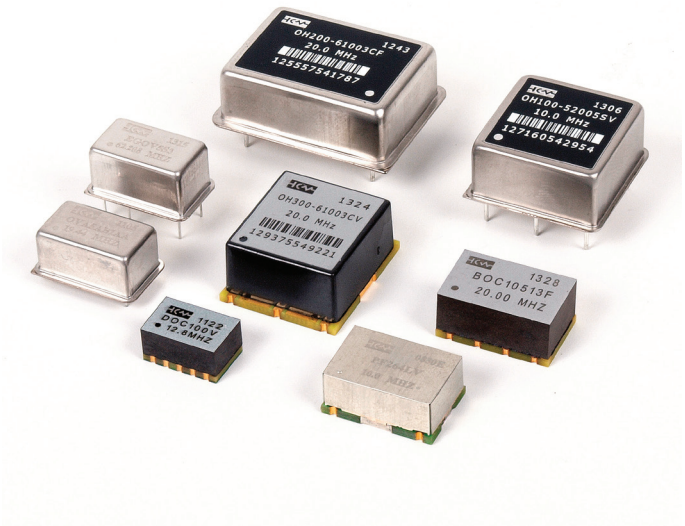
1.2 This document includes the following

- Power and ground circuit design tips.
- Theory of operation / Characterization
- Techniques to achieve optimal thermal conditions using multilayer boards
- A design checklist

1.3 About this document

The methods presented in this application note should be taken as suggestions which provide a good starting point in the design and layout of a PCB. It should be noted that one design rule does not necessarily fit all designs. It is highly recommended that prototype PCBs be manufactured to test designs.

For further information please contact Connor-Winfield Engineering Department.



RoHS COMPLIANT

Application Note	**AN2093**
Page	**1**
Revision	**P01**
Date	**10 May 2013**

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Section 2: Power & Ground Considerations.

2.1 Power Supply and Grounds.

All system designs have a power supply and ground circuit that is shared by all of the components on the board. The operation of one component can affect the operation of other components that share the same power supply and ground circuit.

2.2 Power Supply.

The goal of a system's power supply is to maintain a stable voltage within a specified range while supplying sufficient current. While an ideal power supply would maintain the same voltage for any possible current draw, real world systems exhibit the following behaviors:

- A change in current and its associated noise caused by one device affects other devices attached to the same power supply net.
- A change in current draw affects the voltage of the power net.

2.3 Typical Power Supply System.

A typical power supply circuit consists of the following:

- Voltage regulators that maintain voltage stability within a required range while supplying sufficient current to all components served.
- Bulk, decoupling and bypass capacitors.
- Power and supply circuit runners or power supply planes for power distribution to components.
- Local decoupling and bypass capacitors at each supply sensitive component.

2.4 Power Supply Management.

Improper voltage regulation can result in instability of many system components or complete system failure.

Periods of insufficient power are often referred to as "Brown-Outs", where power supply voltage drops to an insufficient level, or "Black-Outs" where power supply voltages totally disappear for a period of time.

For the OCXO to power up and configure properly on initial power-up, Vcc must exceed the maximum power-on reset (VPOR) voltage in order for the device to proceed with configuration and initialization. The VCC voltage is internally monitored on power-up to properly trigger the device configuration circuitry.

On subsequent brown-out conditions where the device is not power-cycled (i.e., the supply voltages are not take down to 0v), the Vcc voltage must be taken down below the minimum VPOR voltage in order to clear out the device configuration content. Subsequently, the voltages must exceed the VPOR voltage once again in order for the device to be programmed with the new configuration.

A brown-out condition is defined by the Vcc rail dropping below its respective data retention voltage defined by the VRAM in the data sheet.

Please refer to the OCXO data sheet for the minimum and maximum VPOR voltages and Data Retention Voltages.

Prevent system malfunction during periods of insufficient power supply voltage by using external lower voltage detector logic and supply management circuitry.

2.5 POR/BOR Operation.

The power-on reset occurs when the device is started from a Vss level. The brown-out condition occurs when a previously powered device drops below a specified range.

The devices RAM retention voltage (VRAM) is lower than the VPOR/VBOR voltage trip point. When VPRO/VBOR < Vcc < 2.7V, the electrical performance of the OCXO will NOT meet the data sheet specifications.

2.6 Power-on Reset.

When the device powers up, the device Vcc will cross the VPOR/VBOR voltage. Once the Vcc voltage crosses the VPOR/VBOR voltage the following will occur:

- Volatile registers are loaded with values form the corresponding non-volatile registers.
- The TCONF register will load the factory programming.
- The device is capable of Digital / Analog operation.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

2.7 Brown-Out Reset.

When the device powers down, the device Vcc will cross the VPOR / VBOR voltage. Once the Vcc voltage decreases below the VPOR / VBOR voltage the following occurs:

- Factory serial programming interface is disabled.
- Non-Volatile register are no longer programmable.

If the VCC voltage decreases below the VRAM voltage the following occurs:

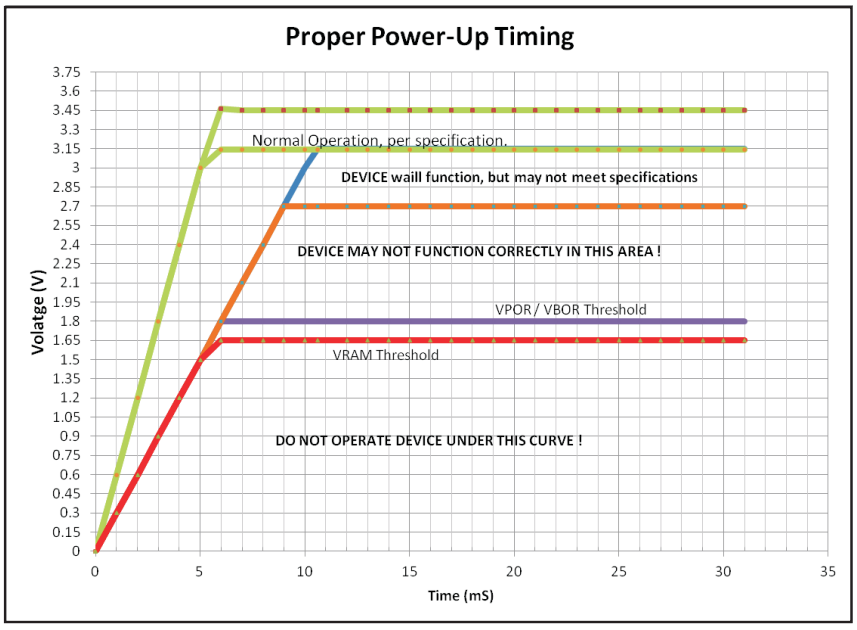
- Volatile registers may become corrupted.
- TCONF register may become corrupted.
- OCXO oven core may lose thermal equilibrium.
- OCXO frequency stability may not meet the data sheet specifications.

As the voltage recovers above the VPOR / VBOR voltage see section “Power-on Reset”
On subsequent brown-out conditions where the device is not power-cycled properly (i.e., the supply voltages are not taken down to 0V), the power supply voltage must be dropped below 1.6 volts in order to clear out the EEPROM device configuration content.

2 8 Voltage Regulators.

A voltage regulator takes an input voltage from an external source and steps it down to a suitable voltage level that can power components on the circuit board. Two common types of voltage regulators are dc-dc converters and low-dropout regulators (LDO). When deciding on a voltage regulator, always review the regulator data sheets to match component specifications with system requirements.

As digital logic gates of ICs switch from one state to another, the IC’s current draw fluctuates at a frequency determined by the logic state transition rate or “rise-time”. These current oscillations cause the power supply voltage to fluctuate as a small voltage develops across the net due to its intrinsic impedance. The circuit’s impedance can be lowered by carefully selecting a capacitor that provides a low-impedance path to ground for high frequencies. As a capacitor charges or discharges current flows through it which itself is restricted by the internal resistance of the capacitor. This internal resistance is known as Capacitive Reactance and is given the symbol XC in ohms. Unlike resistance which has a fixed value, ie 100Ω, 1kΩ, etc. Capacitive Reactance varies with frequency so any variation in frequency will have an effect on the capacitor. The loop from the voltage supply pin to decoupling capacitor to ground should be kept as small as possible by placing the capacitor near the power supply pin and ground pin of the device.



CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

2.9 Low-Dropout Regulators.

Low-Dropout Regulators (LDOs) are less efficient than dc-dc converters, but they also introduce significantly less noise into the power circuits.

2.10 Power Supply Bulk Decoupling and Bypassing.

Noise can be introduced into the power circuit from the voltage regulator, from ICs connected to the net, and from electromagnetic noise that couples into the power supply trace and planes. Power supply "bulk" decoupling capacitors help to minimize the effects of noise and provide other benefits to the circuit as well. Large value bulk capacitors improve performance during low frequency fluctuations in supply current draw by providing a temporary source of charge. Many voltage regulators maintain their voltage by using a negative feedback loop topology that can become unstable at certain frequencies. A capacitor placed at the regulator's output can prevent the voltage supply from becoming unstable. Check the regulator's manufacturer data sheet for recommended capacitor specifications. Bulk decoupling capacitors should be placed as close as possible to the output pin of the voltage regulator.

2.11 Ground Circuits.

The ground circuit can introduce noise to an embedded system and affect components. An ideal ground circuit is "equipotential", meaning that the voltage of the circuit does not change regardless of the current. Real-world ground circuits have a characteristic impedance and experience changes in voltage with changes in current. Careful PCB design can minimize this non-ideal behavior to create a ground circuit that provides a low impedance return path for current.

2.12 Designing with a Ground Plane.

While some systems connect components to a ground circuit through wires or traces most designs use a ground plane in which the PCB's components connect their ground pins to a common conductive plane. Designing with a ground plane is highly recommended for two reasons:

- The return current noise of one device has less effect on other components when sharing ground in a parallel configuration.
- Short connections to ground minimize current return path inductance, which can induce large voltage swings in ground.

2.13 Ground Plane Fill.

A ground plane should cover as much of the board as possible, even in spaces between devices and traces.

"Islands" of copper formed between traces or devices should always be connected to ground and should never be left floating. Spreading the ground plane across the board also aids in noise dissipation and shields traces.

Caution! Care must be taken to thermally isolate the OCXO from the underlying power and ground planes to ensure the OCXO can reach thermal equilibrium. Separating the analog current return path from the noisier digital current return path can improve analog measurements. Ground isolation can also improve performance in boards connected to industrial or noisy systems. Separate ground planes should be connected in only one location, usually near the power supply.

"Caution! Care must be taken to thermally isolate the OCXO from the underlying power and ground planes to ensure the OCXO can reach thermal equilibrium."

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Section 3: Theory of Operation / Characterization.

3.1 OCXO Theory of operation.

The OCXO encloses a crystal in a temperature-controlled chamber called an oven. Frequency stability is achieved by maintaining tight temperature control of the crystal within the oscillator oven. Care must be taken not wick thermal energy away from the OCXO preventing the core from reaching thermal equilibrium.

When an OCXO is turned on, it goes through a ‘‘warm-up’’ period while the temperature of the crystal in the internal oven stabilizes at a temperature significantly warmer than ambient.

During “warm-up”, the performance of the oscillator will not meet the specified frequency stability until normal operating temperature is reached. After the oven has “bridged” the temperature within the oven remains constant as ambient varies.

The oven controller operates such that if the internal temperature of the oven decreases due to an ambient temperature drop, the oven controller will provide more power to compensate for thermal losses. Similarly, an increase in ambient temperature causes a reduction in applied power into the oven and the compensation temperature decreases.

In most modern designs additional heat is considered a problem and will cause most devices to degrade in performance or eventually fail. The heat generated within the OCXO oven core is used to maintain a constant temperature at the crystal.

“During “warm-up”, the performance of the oscillator is degraded until normal operating temperature is reached.”

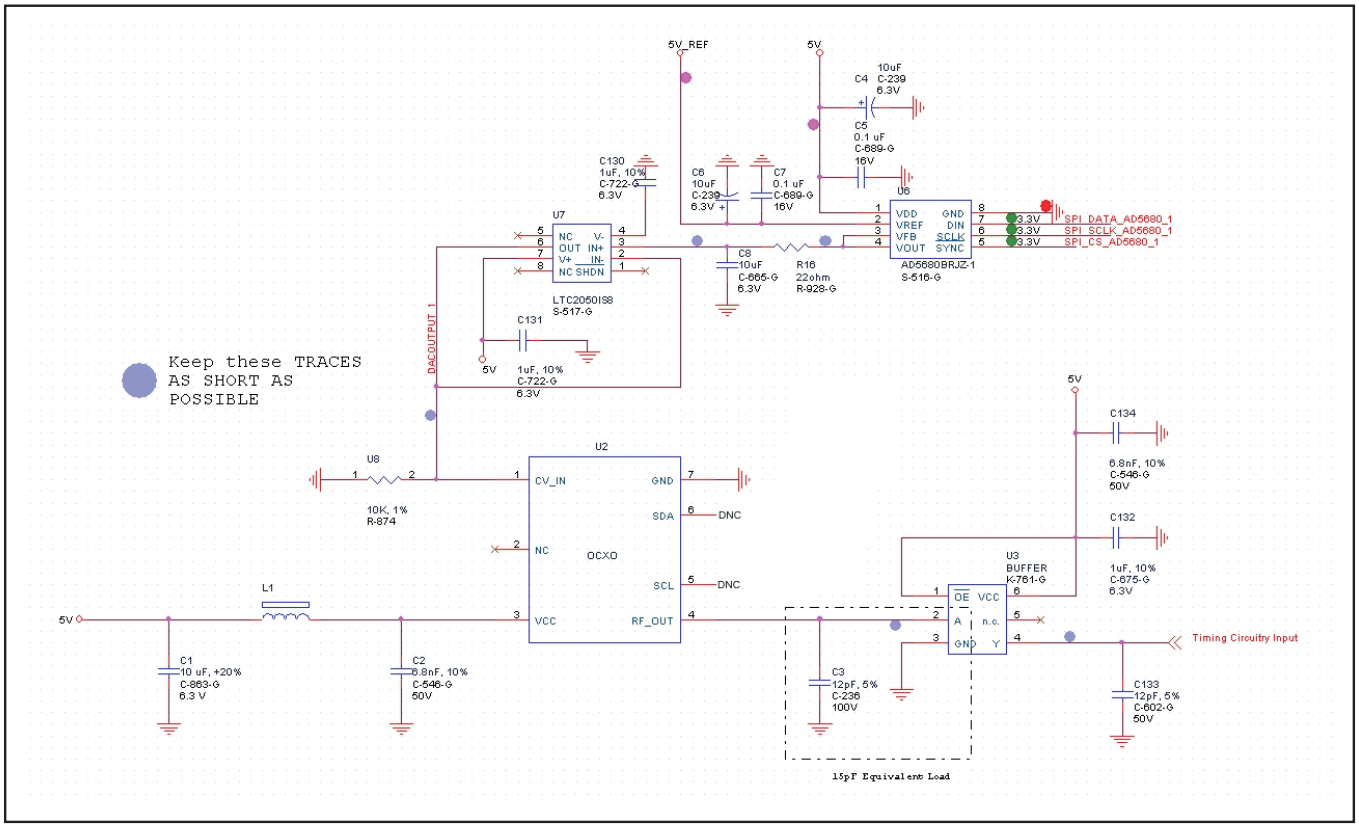


Figure: 5-01

For further information please contact Connor-Winfield Engineering Department.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Thermal Performance Characteristics.

Test Conditions: OCXO mounted in socket, VCC=3.3V, Temperature = @25°C unless otherwise noted.
The following graphs represent the typical characteristics of a DOC052F-010.0MHz OCXO.
Consult with Connor-Winfield Engineering Department for characterization data on any of our existing models.

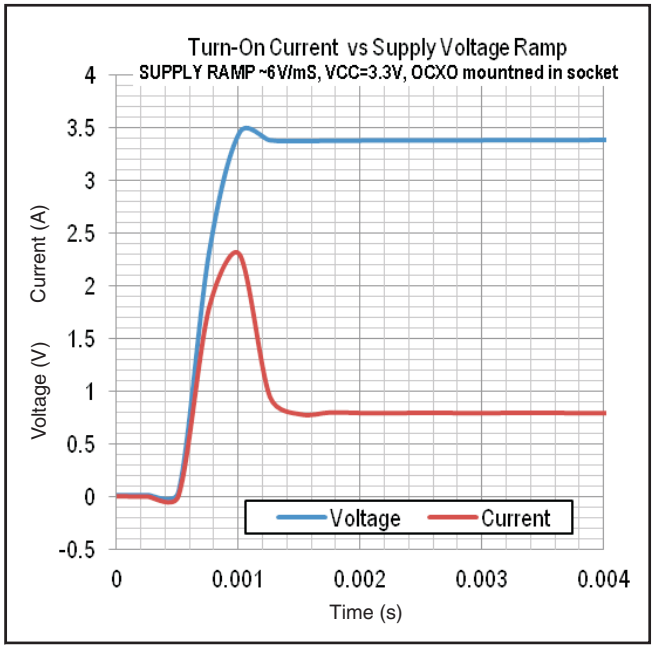


Figure: 6-01

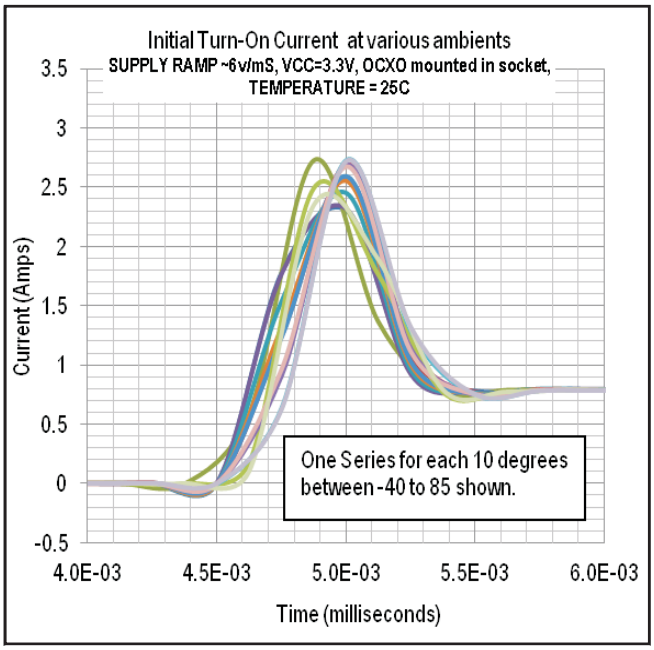


Figure: 6-02

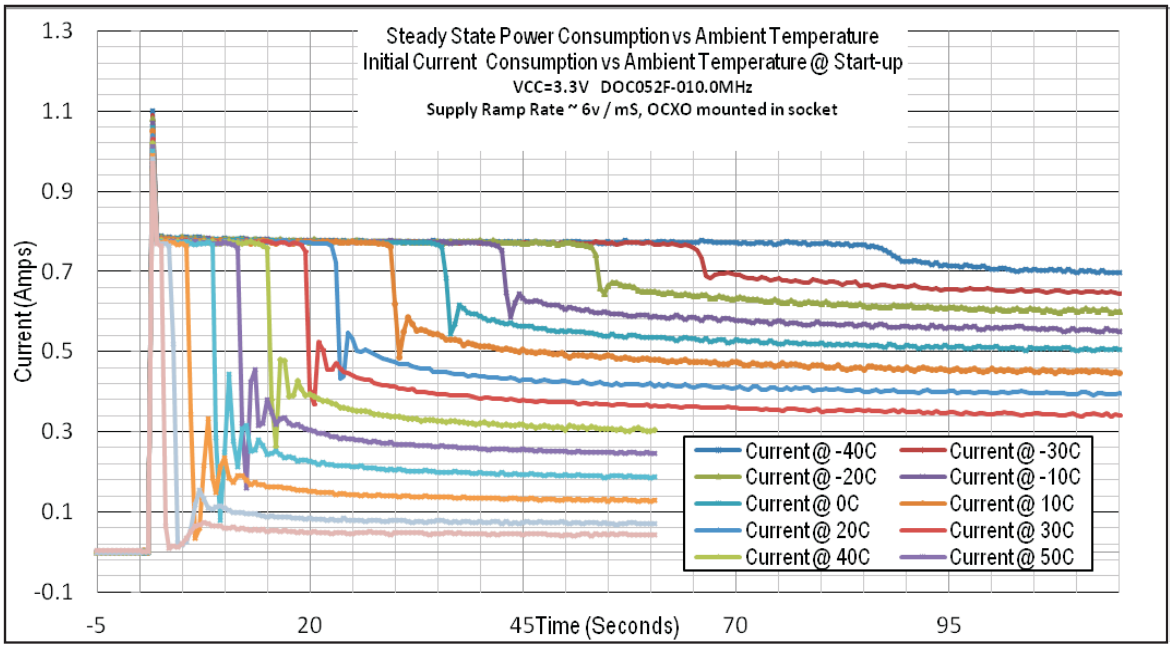


Figure: 6-03

Application Note	**AN2093**
Page	**6**
Revision	**P01**
Date	**10 May 2013**

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Thermal Performance Characteristics.

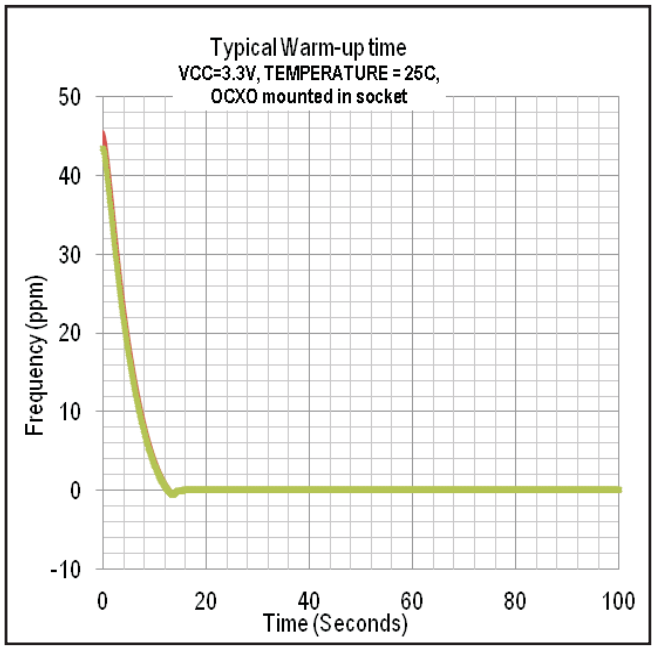


Figure: 7-01 Typical Warm-up Time (seconds)

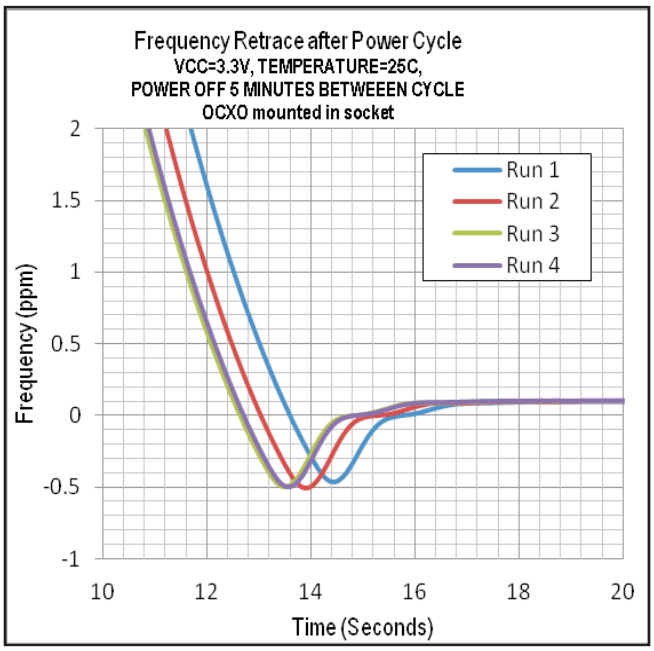


Figure: 7-02 Retrace after power cycle.

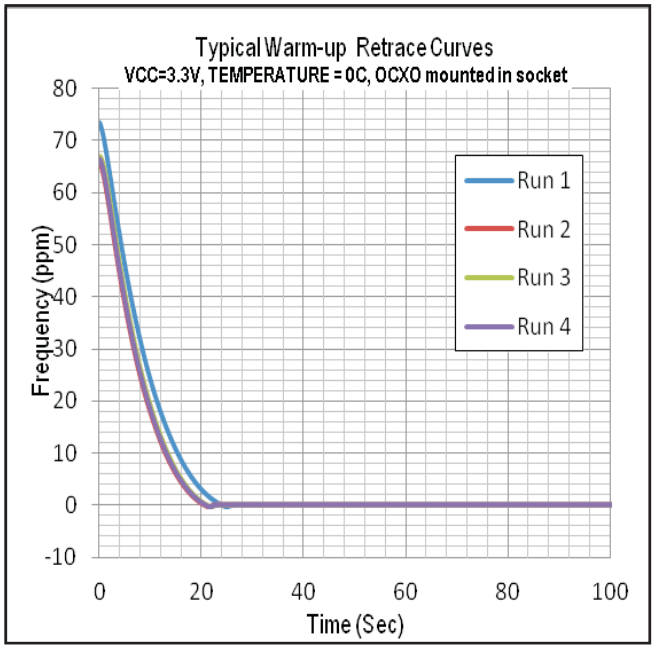


Figure: 7-03 Typical Warm-up Time (seconds)

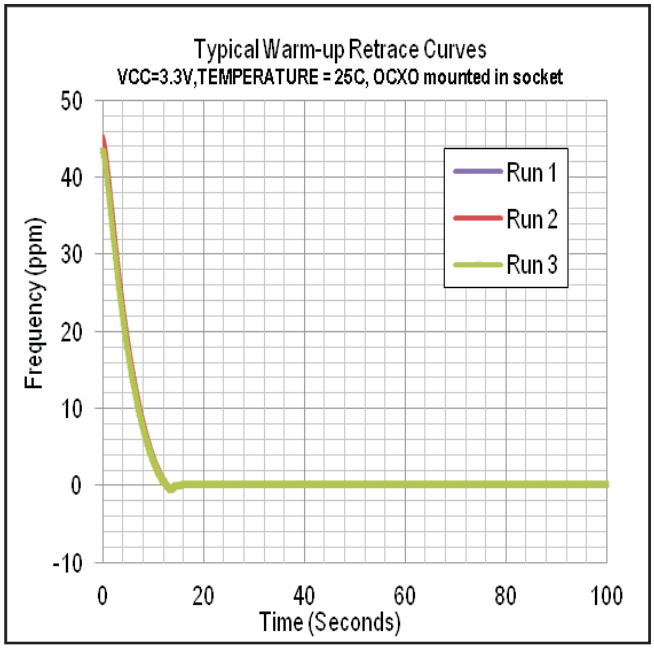


Figure: 7-04 Typical Warm-up Retrace Curves

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Thermal Performance Characteristics.

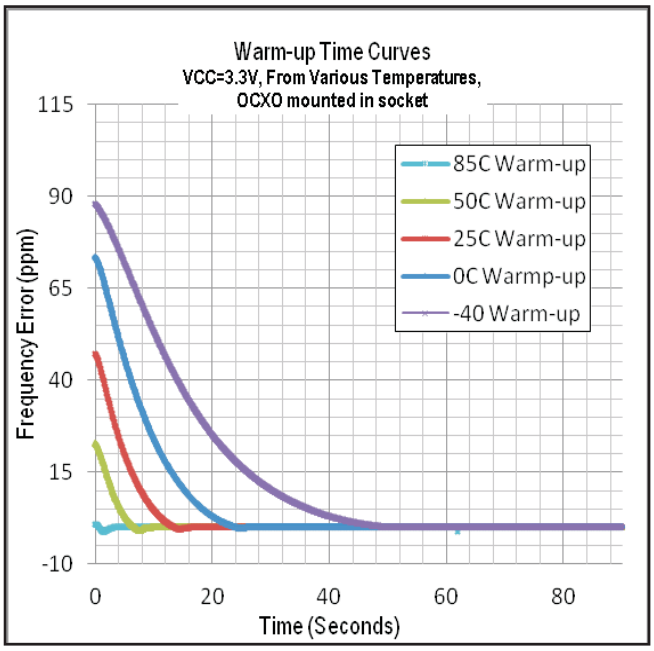


Figure: 8-01 Typical Warm-up Retrace Curves

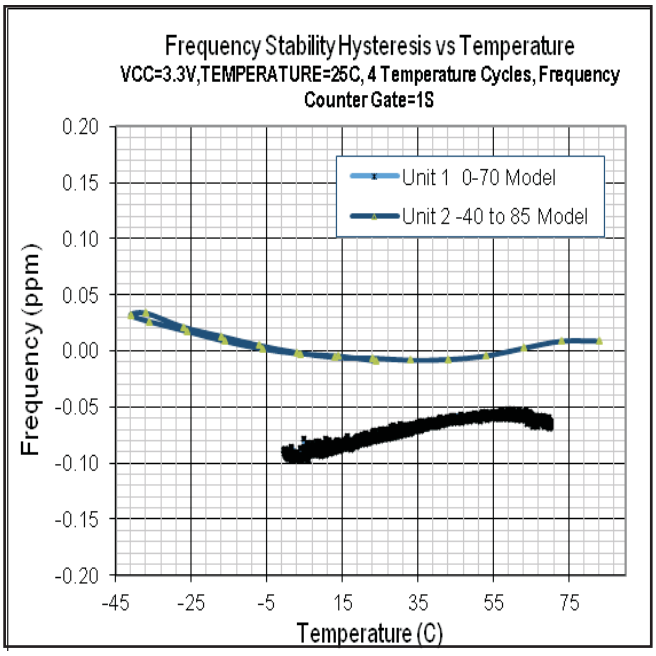


Figure: 8-02 Typical Oscillator Output Start Time

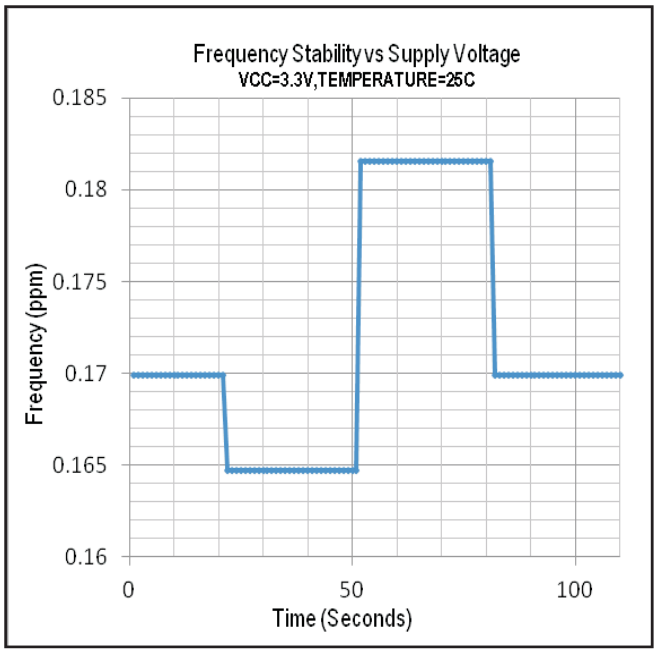


Figure: 8-03 Frequency Error vs Supply Voltage drift (nom, +5,-5,nom)

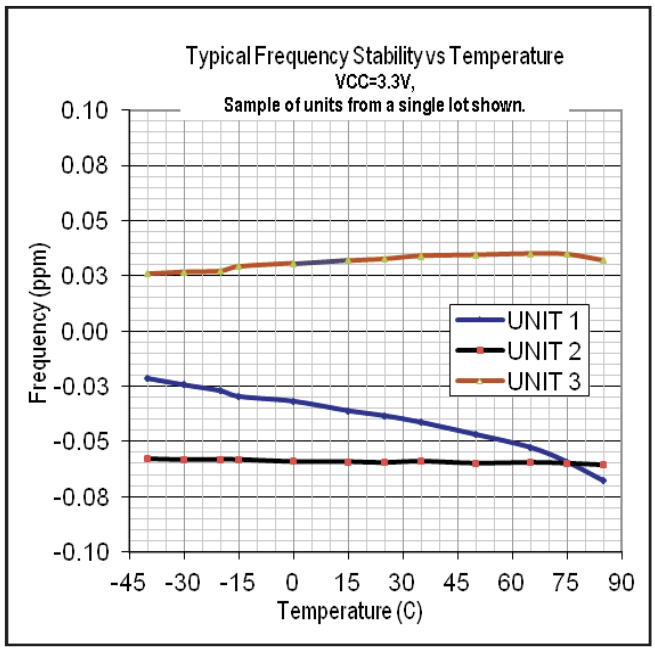


Figure: 8-04 Typical Frequency Stability vs Temperature

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Thermal Performance Characteristics.

Test Conditions: OCXO mounted on 0.062" 6 layer board, VCC=3.3V, Temperature = @25°C unless otherwise noted.
The following graphs represent the typical characteristics of a DOC052F-010.0MHz OCXO.
Consult with Connor-Winfield Engineering Department for characterization data on any of our existing models.

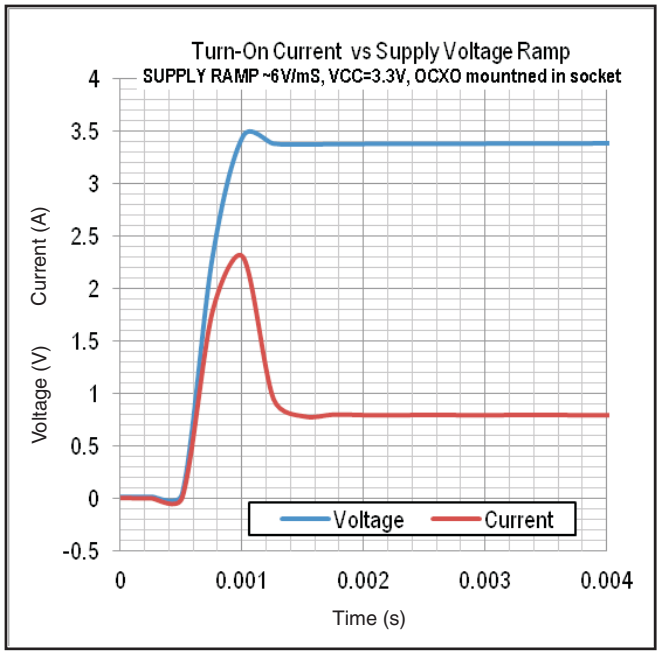


Figure: 9-01

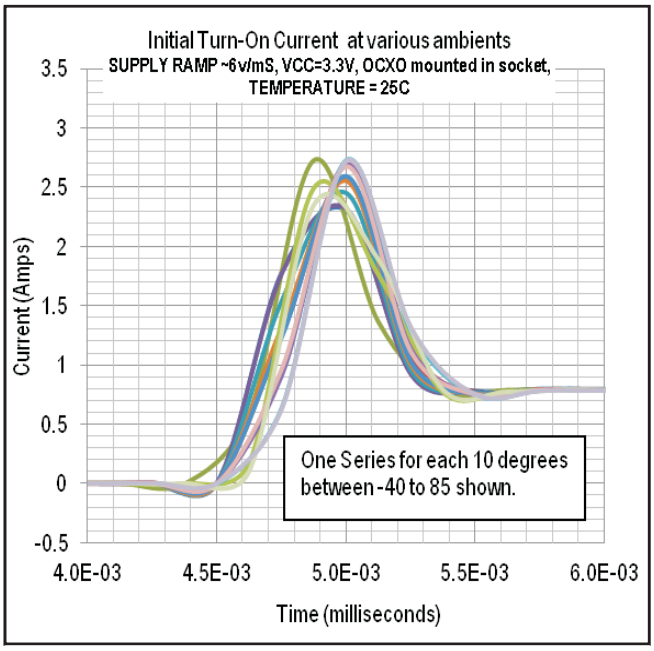


Figure: 9-02

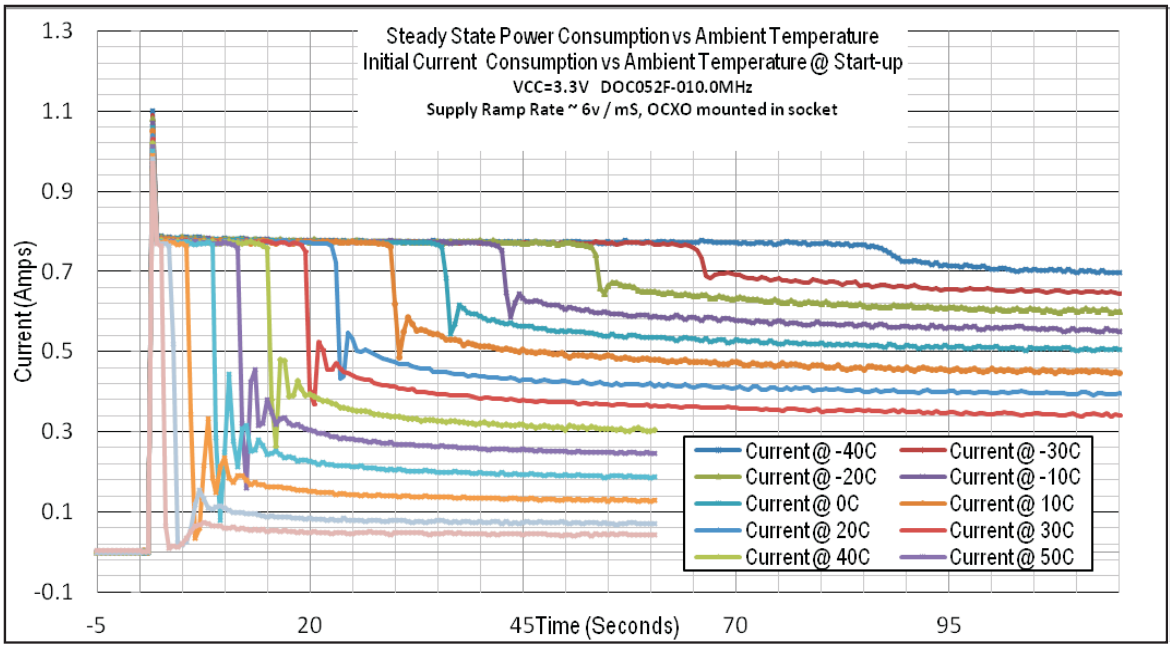


Figure: 9-03

Application Note	**AN2093**
Page	**9**
Revision	**P01**
Date	**10 May 2013**

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Thermal Performance Characteristics.

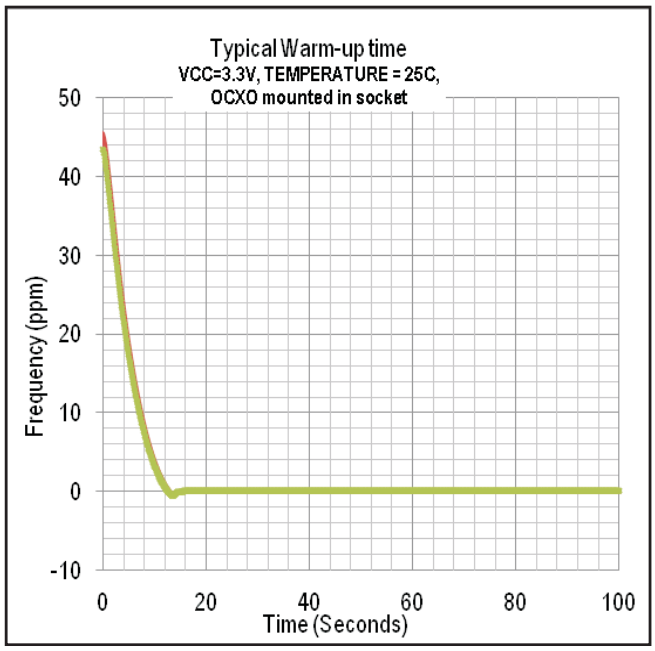


Figure: 10-01 Typical Warm-up Time (seconds)

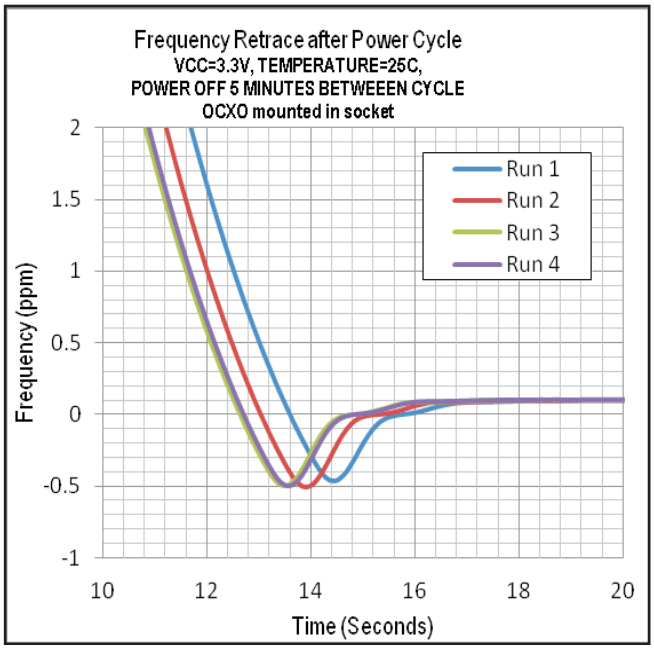


Figure: 10-02 Retrace after power cycle.

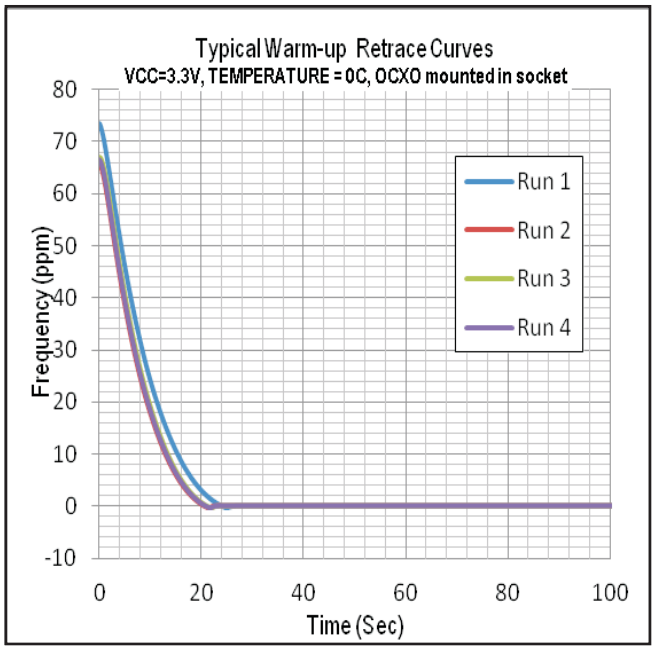


Figure: 10-03 Typical Warm-up Time (seconds)

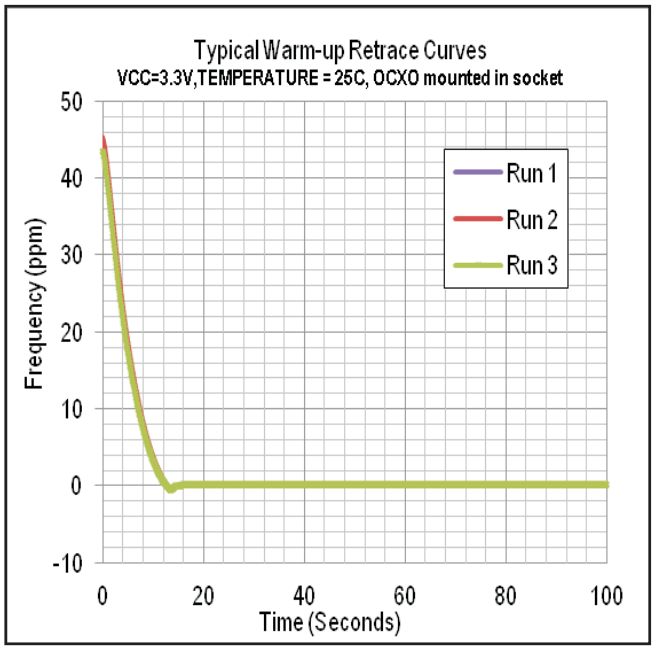


Figure: 10-04 Typical Warm-up Retrace Curves

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Thermal Performance Characteristics.

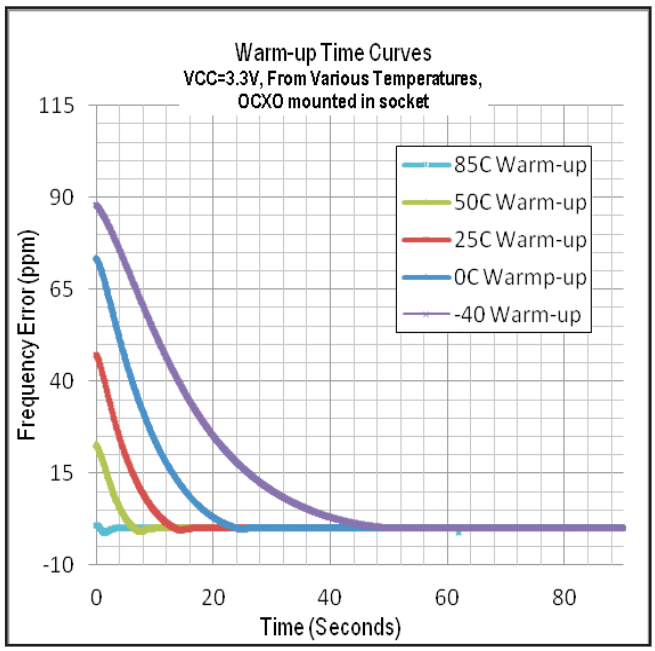


Figure: 11-01 Typical Warm-up Retrace Curves

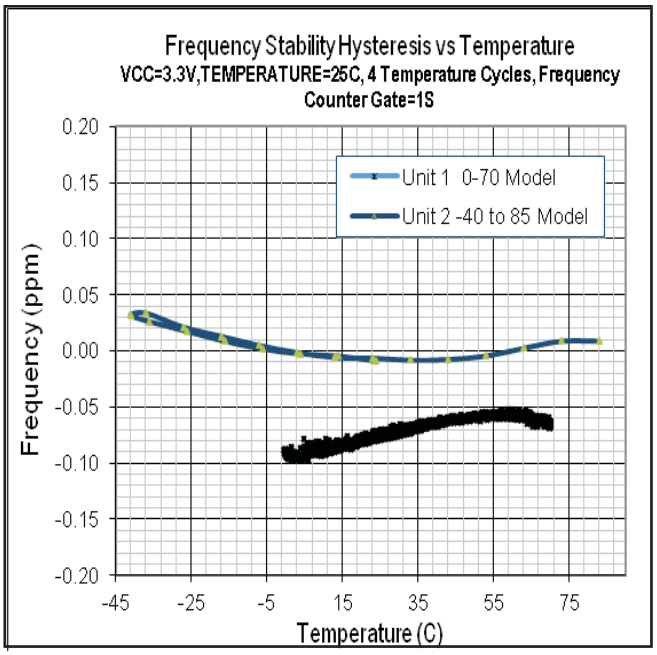


Figure: 11-02 Typical Oscillator Output Start Time

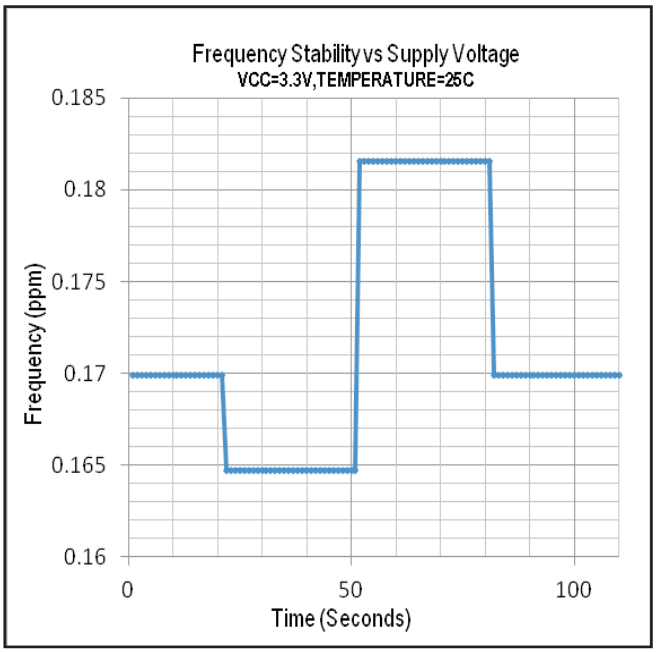


Figure: 11-03 Frequency Error vs Supply Voltage drift (nom, +5,-5,nom)

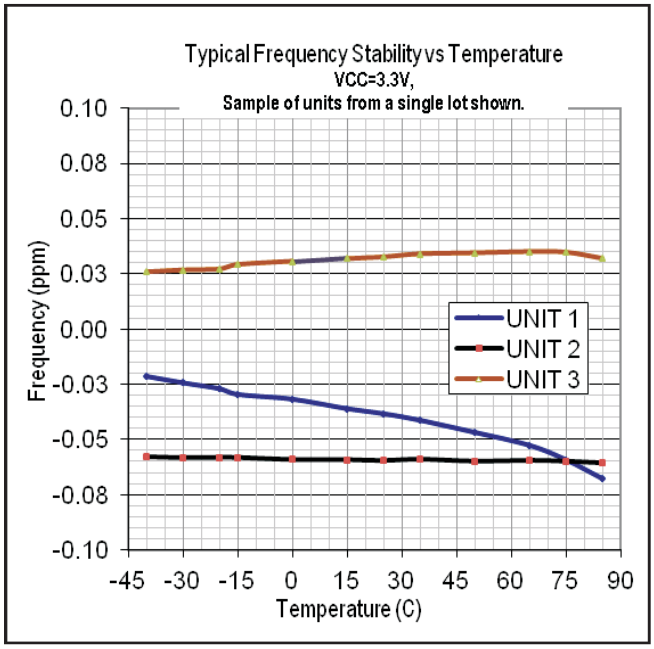


Figure: 11-04 Typical Frequency Stability vs Temperature

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Electrical Characteristics

Test Conditions: OCXO mounted on 0.062" 6 layer board, VCC=3.3V, Temperature = @25°C unless otherwise noted.
The following graphs represent the typical characteristics of a DOC052F-010.0MHz OCXO.
Consult with Connor-Winfield Engineering Department for characterization data on any of our existing models.

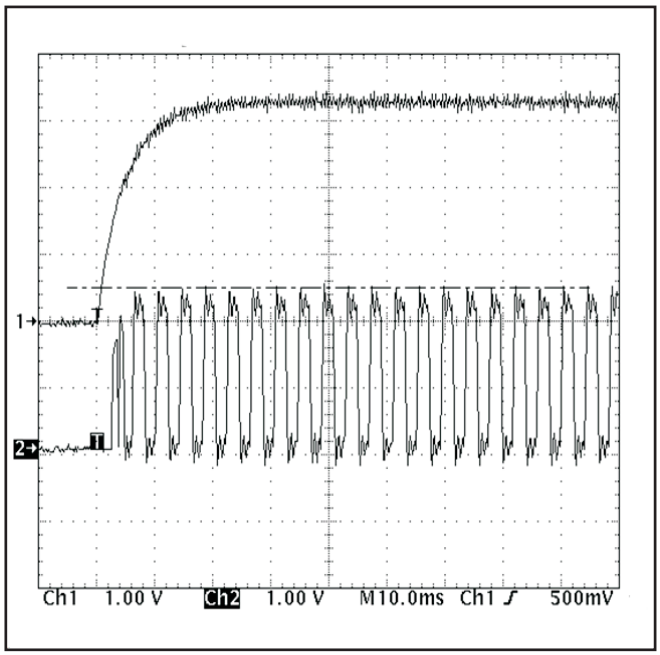


Figure: 12-01 Typical Oscillator Output Start Time

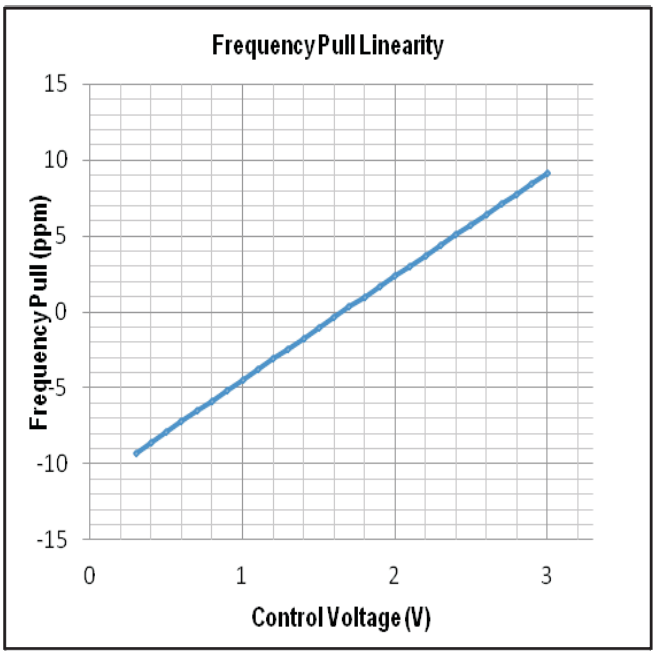


Figure: 12-02 Control Voltage Tuning Linearity

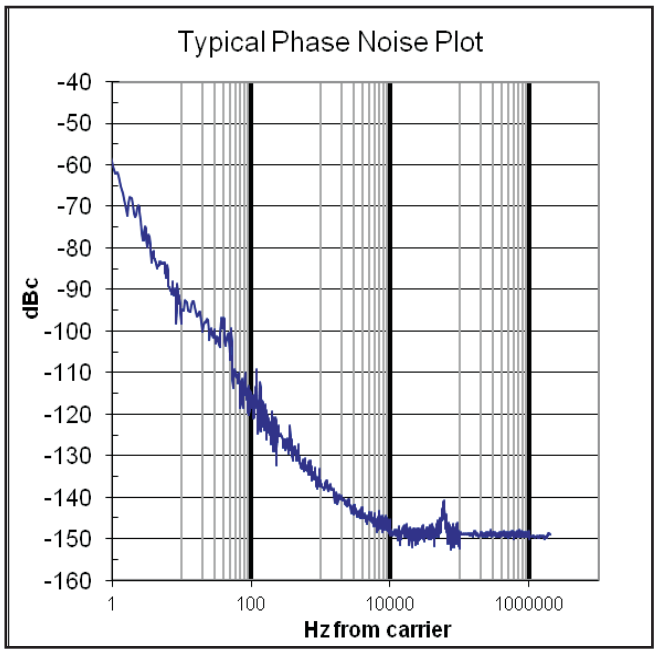


Figure: 12-03 Typical Phase Noise Plot

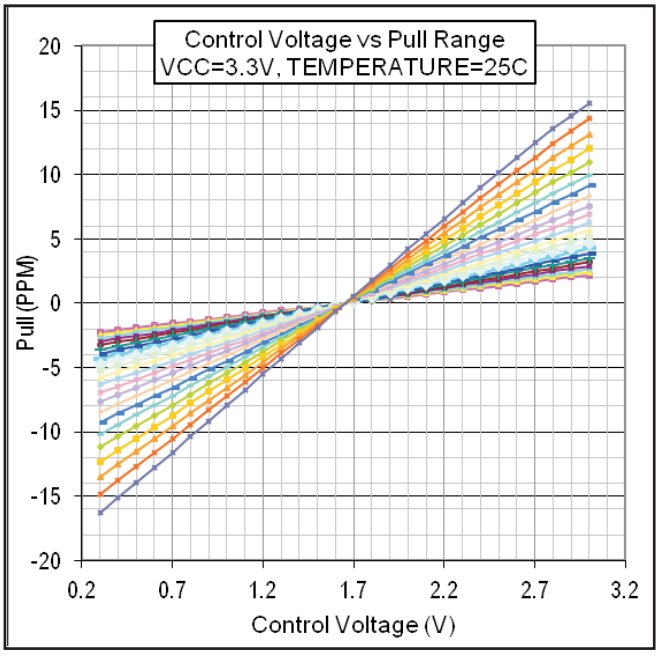


Figure: 12-04 Available Tuning Slopes

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Typical Electrical Characteristics

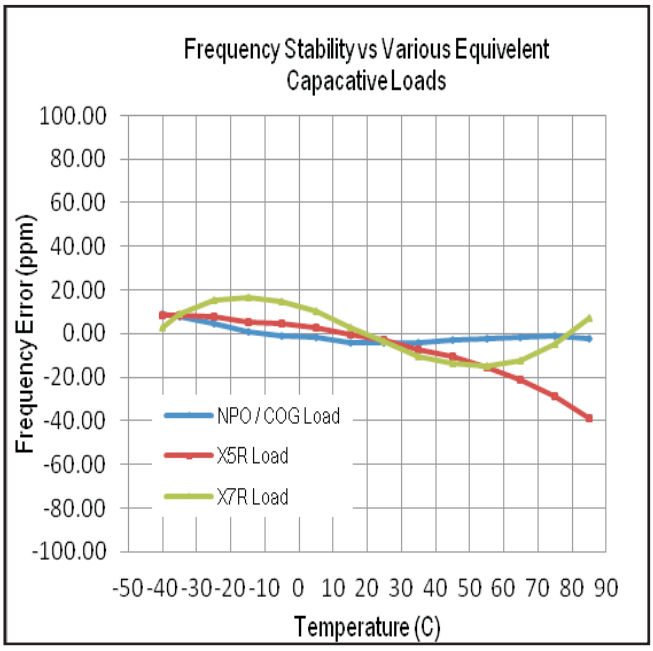


Figure: 13-01

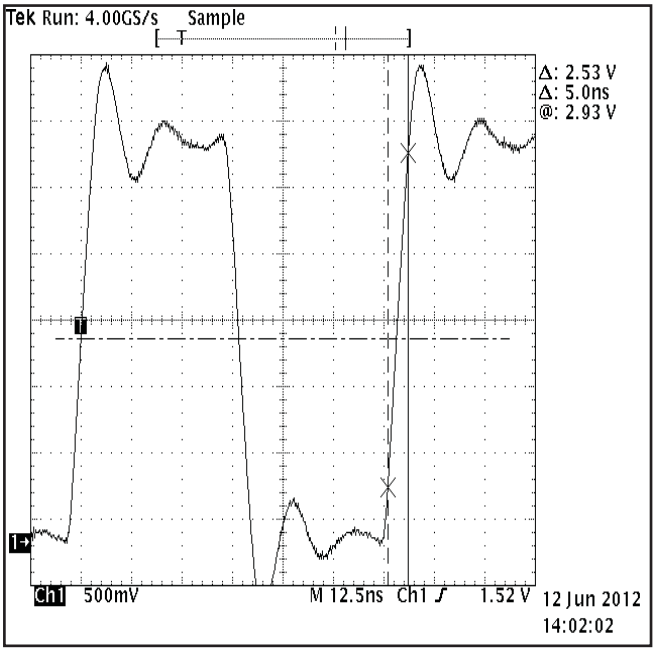


Figure: 13-02

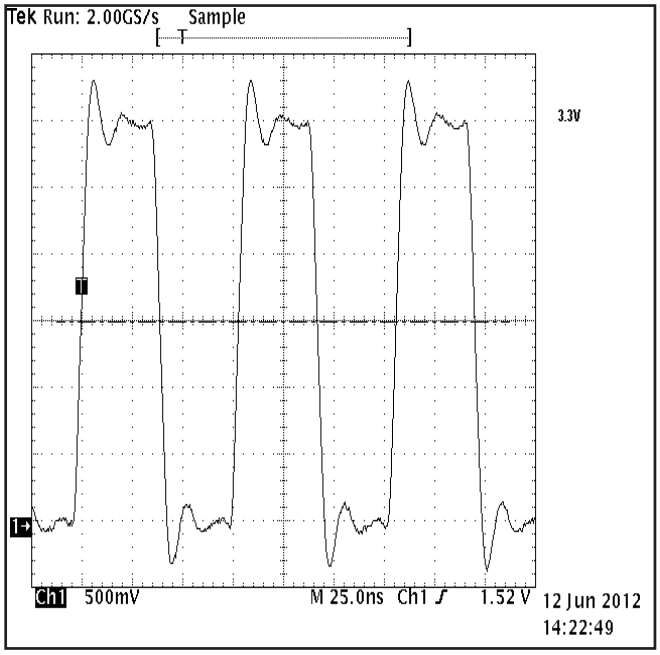


Figure: 13-03

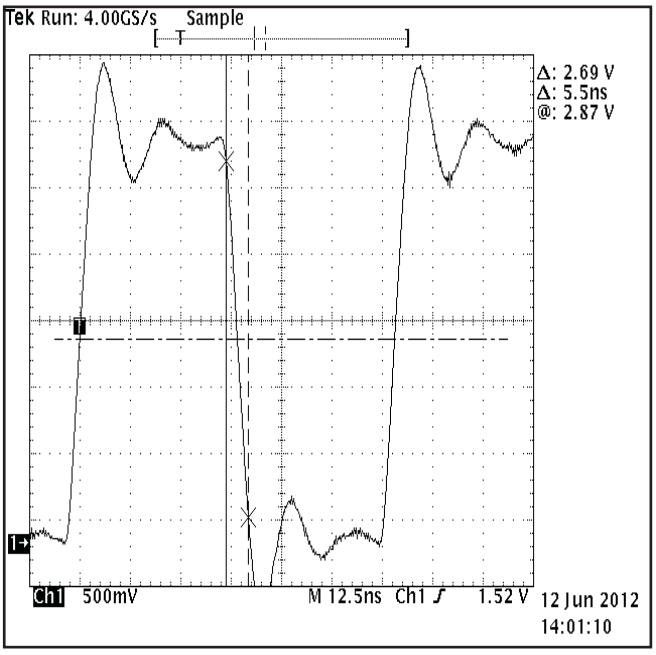


Figure: 13-04

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Section 4: Multi-Layer Board Design / Thermal Considerations

4.1 Layout Considerations

To achieve the stated frequency stability specifications the OCXO must be able to reach and sustain thermal equilibrium over ALL operating conditions. Observation of the ambient operating temperature range, controlled air flow, thermal ramp rates and minimizing thermal energy gains/losses are critical for a successful layout.

"Any attempt to cool, or disperse this heat will cause oven core temperature to drift and OCXO will not meet the specified frequency stability. Improper board layout could also allow heat transfer from nearby components to overheat the oven core resulting in loss of specified frequency stability."

Several thermal design parameters must be carefully considered.

- Board Layout Considerations
- Controlling Thermal Transfer/Transients
- Controlling Air Flow

4.2 Board Layout Considerations

Careful selection of layer stack-ups, ground fills, and trace routing is highly recommended for a successful layout.

"To achieve the stated frequency stability the OCXO must be able to reach and sustain thermal equilibrium over ALL operating conditions"

Consider the following layout concerns.

1. Always place the OCXO near the timing circuitry, and keep all Power / Ground and RF traces as small as possible.
2. Always adhere to stated loading specifications} for OCXO RF output. OCXOs are load sensitive and require an equivalent load capacitor with a flat capacitance vs. temperature curve to achieve stated frequency stability specifications. Consider NPO/COG capacitors when practical for optimal temperature characteristics. See FIGURE 13-01 Frequency Response to various equivalent capacitive loads.
3. Use secondary buffers to fan the OCXO RF signal to multiple inputs or timing circuits. Avoid designs that would "switch in" additional capacitive loads. Avoid designs that would "switch between" multiple capacitive loads. OCXOs are load sensitive devices. See FIGURE XXX
4. Always use speed rated level translators or buffers in applications requiring communication between digital devices operating from multiple supply voltages. Never use resistor divider networks on RF signals.
5. It is recommended to place a 10uF to 47uF bulk capacitor as close to as possible to the VCC pin of the device.
6. Place a small ceramic decoupling capacitor typically NPO/COG/X7R with a 2 to 3 ohm reactance at the output frequency of the OCXO to shunt any noise on the supply rail to ground. Additional decoupling capacitors can be used to filter out other unwanted supply noise generated from other devices.
7. Avoid using series current sense resistors in OCXO monitoring applications. Improper selection of resistor values could create significant voltage drops when combined with the thermal coefficients of the supply, and large current draw from the OCXO.
8. Careful evaluation of via size should be considered with all high power devices to guarantee sufficient current. Maximum current through a via calculations should be made using highest expected board temperature instead of maximum ambient temperature as heat generating components will typically heat the board well beyond the ambient temperature range of the OCXO. Improper via size selection could cause current starvation issues which would result in current oscillations as the oven core is starved of power and unable to reach thermal equilibrium. Via to pad stringers or runners should also be evaluated for sufficient current carrying capacity at maximum expected board temperatures. Via in pad work best, but adds additional board cost.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Multi-Layer Board Design / Thermal Considerations

Free via size calculations tools are available online. Saturn PCB Design Inc. offers this free tool available at the following URL.

http://saturnpcb.com/pcb_toolkit.htm

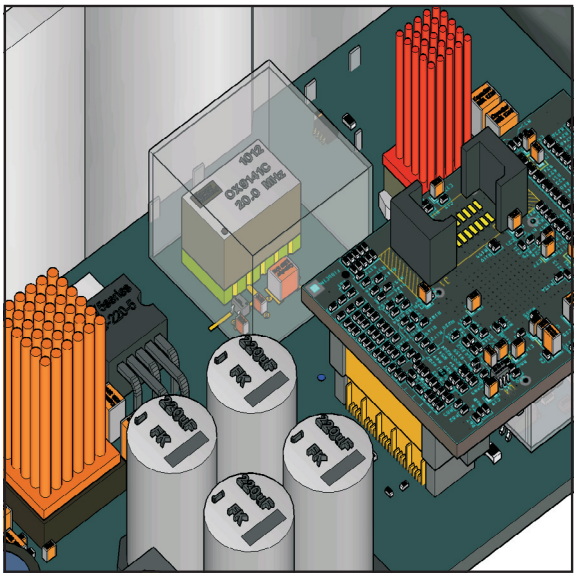


Figure: 15-01

9. Low impedance power and ground planes should be used instead of stringer traces or star based power distribution methods to reduce induced voltages caused by high current devices such as OCXOs.
10. For control voltage equipped models it is important to connect the ground of the control voltage source as close as possible to the OCXO ground to minimize trace impedance and therefore minimize any generated voltages which could cause large frequency errors. It is highly recommended to use the supplied OCXO VREF source to derive the control voltage when equipped. For models that do not offer the OCXO VREF source it is also recommended that the control voltage source run off the same rail as the OCXO to eliminate the supply voltage thermal drift errors that could exist between multiple rails. This will prevent large unwanted frequency shift errors as the relative voltage drift between the supplies will be eliminated. Scenario: Assume a control voltage equipped OCXO with a tuning sensitivity of 7ppm / volt is powered from a 3.3V supply (3V3_OCXOSupply) with a temperature coefficient of 2.6mV / °C.

The DAC which drives the OCXO CV pin is powered from a secondary 3.3V rail (3v3_ DacSupply) with a thermal coefficient of 0.2mV / °C (See Figure 15-02 Example schematic Figure 15-03 Thermal Coefficient vs. Temperature) In this example the OCXO was initially tuned to 0 ppm at 0°C with a calibration error of ± 0.025 ppm. As the ambient temperature in the system changes to 70°C over the next hour, the voltage error between the two rails would have drifted from 0 volts between the two rails, to 0.1834 volts resulting in a 1.2838 ppm frequency error.

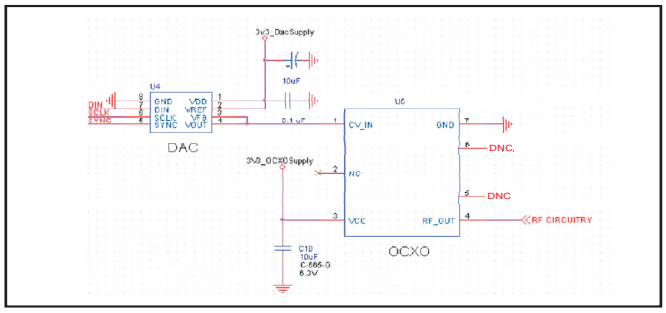


Figure: 15-02 Example Circuit

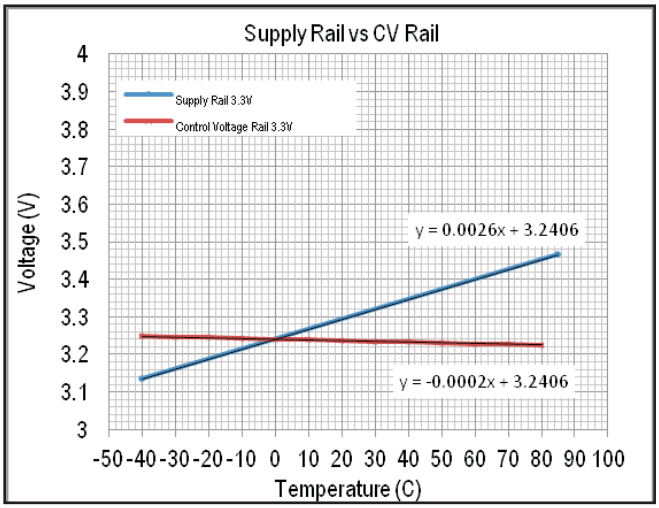


Figure: 15-03 Thermal Drift between Supply Rails

Application Note	**AN2093**
Page	**15**
Revision	**P01**
Date	**10 May 2013**

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Multi-Layer Board Design / Thermal Considerations

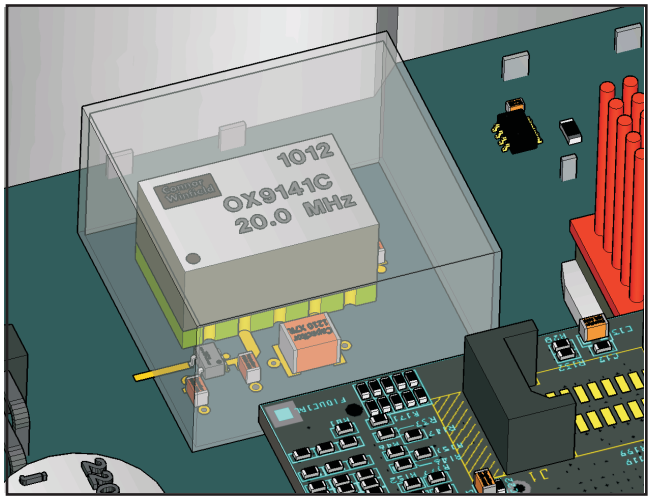


Figure: 16-01

A small air gap should exist between the OCXO and all the walls of the cover.

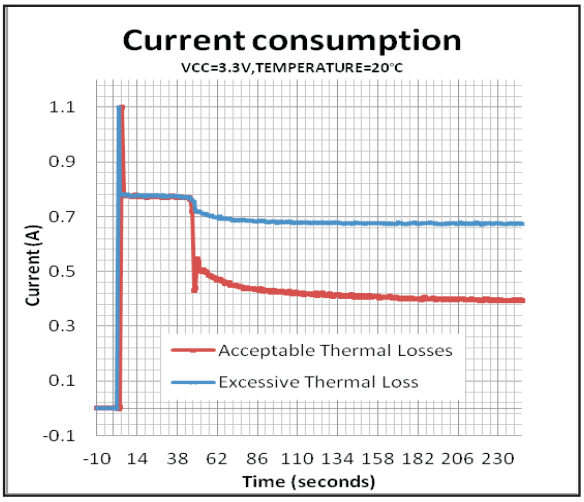


Figure: 16-03

11. To reduce unwanted thermal gains/losses, open a window in any top level copper pours under the device. Excessive thermal losses may result in higher than normal current consumption or complete device failure. See Figure 16-03. Excessive thermal gains will overheat the oven core causing frequency instability. FIGURE 16-02 illustrates a how to properly flood a top layer while creating a "window" under the OCXO.

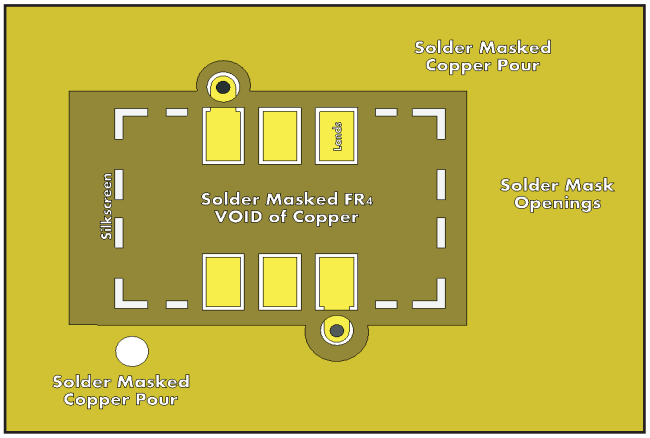


Figure: 16-02
OCXO Pad Layout w/ Top Level Copper pour.

12. Optionally a thermal "moat" can be created to prevent thermal energy transfers between the OCXO and board as seen in Figure 17-01. A thermal moat is a routed area around the OCXO and is very effective means to prevent losses from the oscillator while still allowing a top layer pour on the board to heat sink cool other electrical components.
13. Plastic and metal covers can be used to further reduce small temperature fluctuations in the system by reducing variable air flow across the device. An effective cover will should still allow a small air gap between the OCXO and any wall of the cover. SEE FIGURE 16-01
14. DO NOT CONNECT ANY ELECTRICAL SIGNALS TO PINS MARKED DNC. These pins are reserved for factory use only, and connecting or monitoring these signals could permanently damage the device.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Multi-Layer Board Design / Thermal Considerations

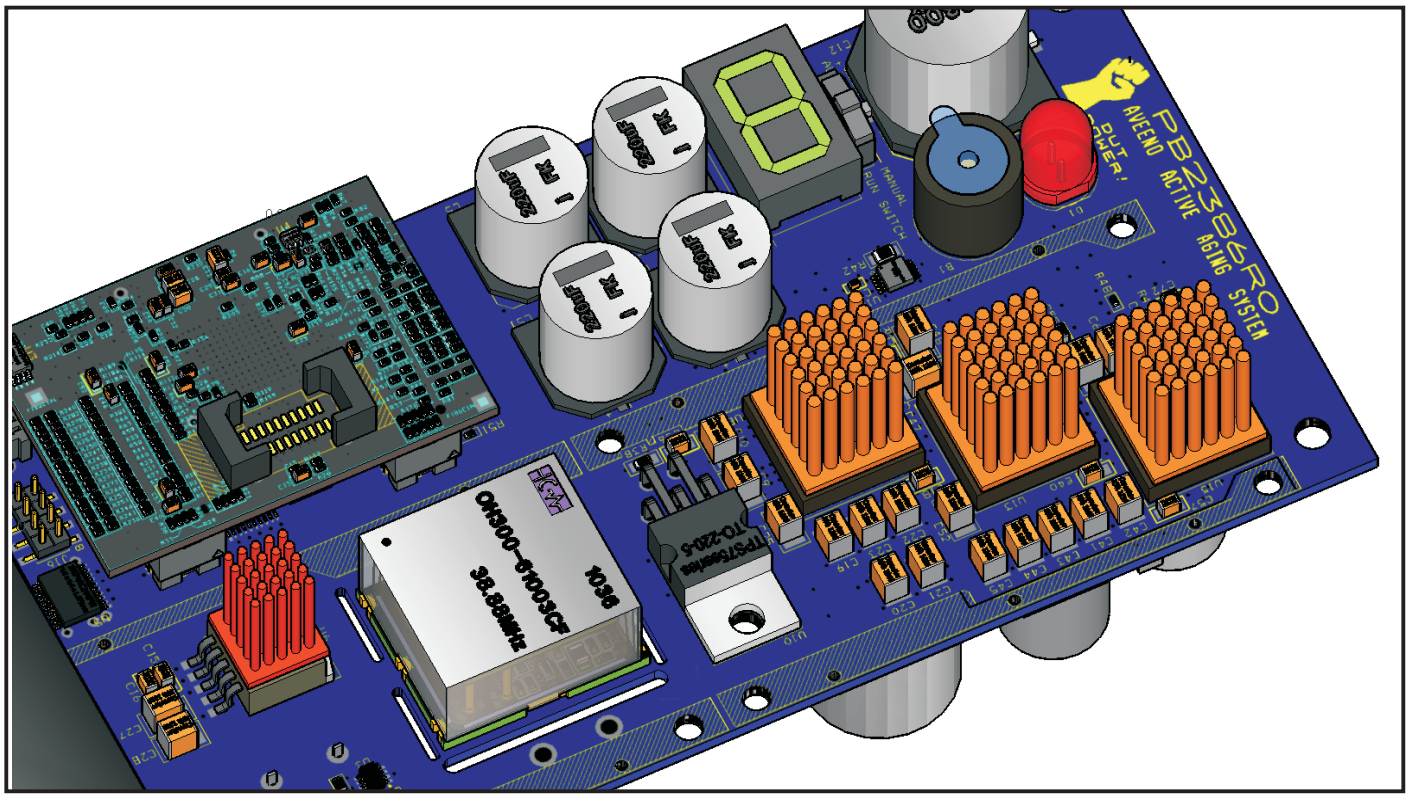


Figure: 17-01

Optionally a thermal “moat” can be created to prevent thermal energy transfers between the OCXO and the surrounding heat generating components.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Multi-Layer Board Design / Thermal Considerations

4.3 Controlling Thermal Transfer / Transients

Controlling thermal transients is critical for proper operation of all OCXOs. Any sudden changes in air-flow, or temperature will drastically effect short term frequency stability. Ambient system, cabinet, or enclosure temperature must always transition under the maximum stated rate identified on the product data sheet. Typical $\Delta t^{\circ}C$ / t (minutes) rates for OCXO range from 0.5 to $1^{\circ}C$/minute. Any additional heat generated by nearby integrated circuits, or mechanical parts could cause the internal oven temperature to fall out of equilibrium and no longer maintain frequency stability. The OCXO controller can only self-regulate oven core temperature if thermal energy conducted through the printed circuit board is kept to a minimum.

Avoid the following, as they will cause the oven core to overheat or drop out of thermal regulation.

- Placing the OCXO near heat generating components (electrical or mechanical that could bleed thermal energy into the OCXO causing the oven core to overheat, even when the ambient air is within the operating limits)
- Placing the OCXO into intermittent air flow paths (ie switched or variable speed fans) as this will cause the oven core to fall out of thermal regulation
- On multi-layer boards avoid top level copper floods, pours and fills under the OCXO land pattern that would contribute to excessive heat gains/losses through the printed circuit board resulting in an inability for the oven core to maintain thermal equilibrium.

Avoid layouts as seen in FIGURE 18-02

4.4 Controlling Airflow

Shielding the OCXO from intermittent or variable speed airflow paths will minimize small temperature fluctuations and substantially improve short / medium term stability. This can best be accomplished by shielding the OCXO behind taller non-heat generating components or mechanical parts to create a physical barrier, or with the use of a metal or plastic cover.

See figures 18-01 and 18-02

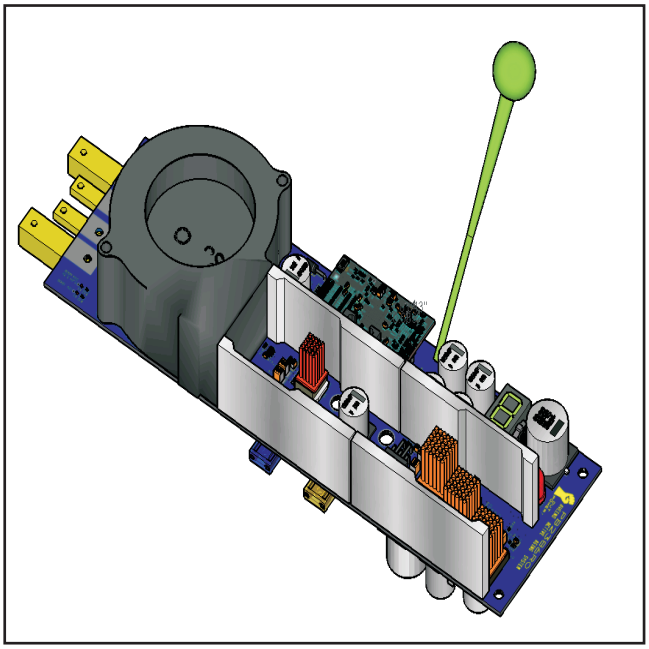


Figure: 18-01

Good Choice for OCXO placement. OCXO is outside of air tunnel, not near any heat generating components

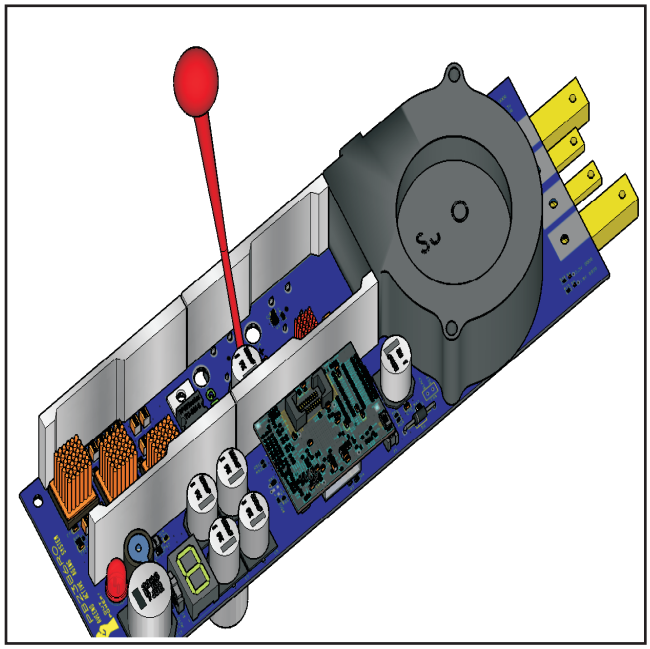


Figure: 18-02

Poor location for OCXO. Variable speed or switched fans create large temperature fluctuations

Application Note	**AN2093**
Page	**18**
Revision	**P01**
Date	**10 May 2013**

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Section 5: Design Checklist

5.1 Power Supply Checklist

- Select a LOW noise power circuit / source
- Add a large bulk capacitor at the voltage regulator's output that can provide current for local capacitors and ensure regulator stability.
- Place bulk capacitors as close to the voltage regulator output as possible.
- The large bulk capacitor's capacitance should be 10 to 100 times as large as local IC decoupling capacitors.
- Add a second capacitor an order of magnitude or two smaller in capacitance relative to the large bulk capacitor to help filter high-frequency noise.
- Place a local capacitance as close as possible to the power supply pin of each IC.
- The side of the local capacitor that connects to ground should be placed as close to the IC's ground pin as possible in order to minimize the loop area between the cap and the power and ground pins.
- Add a filter, such as an L-C filter or an R-C filter, to the power supply circuit.

5.2 Ground

- Design using a ground plane instead of traces when connecting components to ground.
- If a top level copper pour is used, it should cover as much of the board as possible, including the spaces between devices and traces. EXCLUDE THE AREA UNDER THE OCXO.
- Separating the analog ground plane from the digital ground plane improves analog performance.
- Separate ground planes should be connected in only one location, usually close to the power supply.

5.3 General

- Keep analog and digital signals as far apart from each other as possible.
- Avoid routing analog and digital traces perpendicular to each other.
- Avoid routing analog or digital signals under oscillators.
- Trace width should remain constant throughout the length of the trace.
- Turns in traces should be routed using two 45 degree turns instead of one 90 degree turn.
- Trace length should always be minimized.
- Use vias only when absolutely necessary.
- Avoid the use of vias when routing high-frequency signals.
- Keep traces as small as possible.
- Place the OCXO as close as possible to the timing circuitry.
- Never leave the control voltage signal floating.
- Design using a power plane instead of traces routed from the power supply.

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

5.4 OCXO Layout Considerations

- Always place OCXO as close to timing circuitry as possible..
- Always adhere to stated loading specifications for RF output of OCXO and consider using NPO / COG capacitors to create equivalent loading capacitance for optimal capacitance vs. temperature characteristics.
- It is recommended to place a 10uF to 47uF bulk capacitor as close to as possible to the VCC pin of the OCXO.
- Place a small ceramic decoupling capacitor typically X7R with a 2 to 3 ohm reactance at the output frequency of the OCXO to shunt any noise on the supply rail to ground.
- Calculate via size to ensure sufficient current is available to the OCXO at the anticipated maximum board temperature which may be SIGNIFICANTLY higher than ambient air temperature.
- Connect the ground of the control voltage source as close as possible to the OCXO ground to minimize trace impedance.
- Open a window in all ground and power planes under the device. Excessive thermal losses may result in higher than normal current consumption or complete device failure.
- Do not place OCXO in path or turbulent airflow which could cause quickly changing temperature fluctuations that could compromise the oven core temperature.
- [Optional] Route a thermal “moat” to prevent thermal energy transfers between the OCXO and board.
- [Optional] Use plastic and metal covers can be used to further reduce small temperature fluctuations in the system by reducing variable air flow across the device.
- DO NOT connect any signals to “Do Not Connect” (D.N.C.) pins. These are FACTORY use only. DNC pads may be soldered down to electrically isolated pads for structural support only.

Section 6: References

Chester Simpson "Linear and Switching Voltage Regulator Fundamentals"
National Semiconductor http://www.national.com/assets/en/appnotes/f4.pdf

Habeeb Ur Rahman Mohammed, Ph.D " Supply Noise Effect on Oscillator Phase Noise,"
Texas Instruments, Application Report SLWA066–November 2011 http://www.ti.com/lit/an/slwa066/slwa066.pdf